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SPICE Modeling and Performance Analysis of Enhancement-Mode GaN HEMTs for Augmented Hard-Switching Energy Conversion Efficiency

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ABSTRACT

The advancement of renewable energy sources necessitates the development of effective power electronic devices. Enhancement-mode Gallium Nitride (E-GaN) high-electron-mobility transistors (HEMTs), an emerging wide-bandgap semiconductor device, demonstrate potential in photovoltaic (PV) energy converting applications to enhance power transfer efficiency. This paper discusses the enhanced semiconducting characteristics of GaN HEMT over conventional silicon power devices by analyzing spontaneous and piezoelectric polarizations of wurtzite GaN crystalline structure and the formation of two-dimensional electron gas (2DEG). The lateral device structure of E-GaN HEMT and normally switched-on depletion mode GaN HEMT are compared. A device-under-test (DUT) equivalent model incorporating parasitic components is proposed, adopting the EPC2204 Level 3 SPICE model. The model is simulated in a novel Double Pulse Test (DPT) topology with clamping and snubber subcircuits using LTSPICE software. The performance of GaN E-HEMT is compared to a MOSFET with similar parameters, and the impact of parasitic inductances and stray capacitances is evaluated through switching

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analysis. Findings support the potential of E-GaN HEMTs and indicate the DC-DC converter design considerations for portable solar PV system applications.

Keywords: DPT, E-GaN HEMT, parasitic inductance, power electronics, SPICE modeling, switching power losses

INTRODUCTION

Renewable energy development has significant implications for the global environment and economy. Among various sources, solar energy presents a promising solution for diverse applications (Ahmad et al., 2011). The escalating demand for sustainable and efficient energy conversion and transfer has spurred the need for innovative semiconductor devices and technologies in power electronics for renewable energy applications. Nonetheless, conventional silicon-based power semiconductors, such as Metal Oxide Silicon Field Effect Transistors (MOSFETs), which are frequently employed in DC renewable energy power electronic systems, exhibit constraints in power density, on-resistance, temperature resilience, and switching speeds (Roccaforte et al., 2018). These limitations lead to considerable power switching losses and protracted switching response times. To overcome these obstacles, wide bandgap semiconductor devices, especially Gallium Nitride (GaN) and Silicon Carbide (SiC), have emerged as popular substitutes for solid-state device operation under high voltage and power conditions (Chow, 2015; Jones et al., 2016). As illustrated in Figure 1, GaN demonstrates superior material properties in comparison to silicon (Si), encompassing a higher electric critical breakdown field, energy bandgap, saturated electron velocity, and electron mobility.

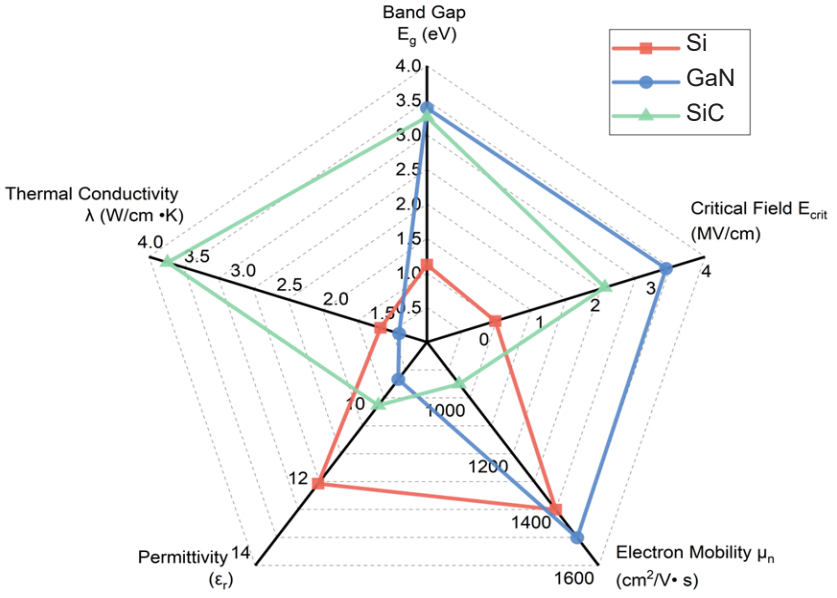


Figure 1. Properties of GaN comparing with Si and SiC

This numerical value in the bandgap signifies the energy level disparity between the valence and conduction bands, closely related to how strong the atomic bonds within the lattice are. These stronger connections imply that it will be more challenging for electrons to move between sites. It leads to lower intrinsic leakage currents and higher operating temperatures for semiconductors with greater band gaps, making it possible for them to have smaller depletion areas and produce device architectures with many carriers. These architectures have little resistance and capacitance because they have smaller transistors and shorter current channels. These qualities enable devices to operate at speeds up to 100 times quicker than those of conventional designs (Lidow et al., 2019). As indicated by the data presented in Figure 1, GaN exhibits a larger bandgap compared to silicon, which is advantageous for high voltage and power applications.

Moreover, the more robust chemical bonds, which contribute to an increased bandgap, also necessitate a greater critical electric field to instigate impact ionization, thereby leading to a heightened breakdown voltage. This relationship can be articulated through the subsequent Equation 1.

$$V_{BD} = \frac{1}{2} w_{drift} \cdot E_{critical} \quad [1]$$

The device's breakdown voltage (V_{BD}) is consequently proportional to the drift region's width (W_{drift}) and the critical breakdown field ($E_{critical}$). GaN could feature a drift area that is an order of magnitude smaller than silicon while maintaining an equivalent breakdown voltage. Carriers must exist in the drift area and be depleted when the device reaches the required field to sustain this electric field. This feature emphasizes a significant benefit for devices with exhibited elevated critical fields. The one-dimensional simplified form of Poisson's equation under constant relative permittivity could be potentially employed to determine the number of electrons between two terminals (presuming an N-type doped device, most carriers are electrons) (Equations 2 & 3).

$$\frac{d^2 V_{BD}}{dw_{drift}{}^2} = -\frac{q \cdot N}{\varepsilon_o \cdot \varepsilon_r} \quad [2]$$

$$q \cdot N = \varepsilon_o \cdot \varepsilon_r \cdot \frac{E_{critical}}{w_{drift}} \quad [3]$$

Within Equations 2 and 3, q represents the electron's charge ($1.602 \times 10^{-19} C$), N denotes the aggregate numbers of electrons in the device dimensions, ε_o signifies the vacuum permittivity ($8.854 \times 10^{-12} F/m$), and ε_r corresponds to the relative permittivity as compared to the vacuum. Under stable direct current (DC) conditions, permittivity is identical to the crystal's dielectric constant. The charge density in the drift area must be much higher, according to the second-order derivative connection between the electric potential and the width of the drift region. This fundamental principle underpins the superior semiconducting performance of GaN over Silicon in power conversion applications. Nonetheless, GaN

exhibits inferior thermal conductivity in comparison to Silicon. Incorporating GaN semiconductors in power electronic applications directed at renewable energy sources requires striking a balance between material attributes to ensure exceptional performance and considerable downsizing of passive and magnetic constituents.

In this paper, the GaN crystalline and the GaN HEMT device structures, including depletion-mode GaN (D-GaN), the gate injection transistor (GIT) E-GaN, and Schottky E-GaN, are primarily introduced. Secondly, the HEMT DUT circuit topology with parasitic components is then developed. Furthermore, LTSPICE simulation software is utilized, integrating the GaN E-HEMT manufacturer model for optimal switching performance analysis against a comparable MOSFET. Finally, the DUT model is combined with the designed DPT circuit to investigate the effects of parasitic inductances and stray capacitances.

PROPERTIES OF GAN HEMT

Wurtzite GaN Polarization and 2DEG Generation

GaN, a widely investigated III-V binary compound wide bandgap semiconductor material, predominantly exhibits a wurtzite crystal structure under standard conditions, making it a prime candidate for semiconducting applications. As illustrated in Figure 2, created using VESTA 3D visualization software, this stable structure, identifiable by its unique hexagonal lattice, leads to superior growth quality and electrical properties, particularly on the c-plane (0001), widely employed in HEMT applications. Alternative planes, such as the non-polar (1120) and semi-polar (1011), offer potential advantages like mitigating piezoelectric polarization effects, thus reducing defect impacts and improving device performance. The inherent polarization of the wurtzite structure contributes to GaN's superior conductivity over silicon, further enhanced by its notable chemical stability and thermal resilience.

Wurtzite GaN compounds exhibit spontaneous polarization due to electronegativity variations in their constituent atoms, which depends on the crystal growth direction. Piezoelectric polarization, on the other hand, arises from mechanical strain when two materials with different lattice constants coalesce. This strain triggers a slight atomic shift within the lattice, creating an electric field. The extent of polarization is directly linked to the in-plane strain and is determined by the mismatch in lattice constants (Wonglakhon & Zahn, 2020).

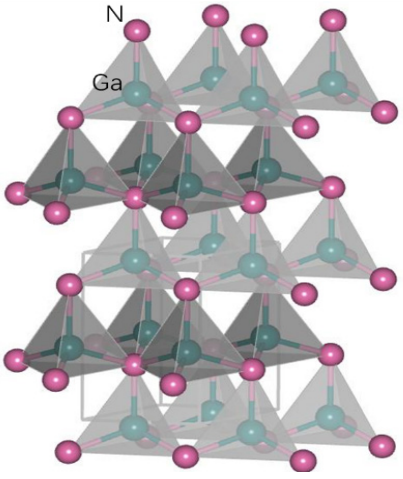


Figure 2. Wurtzite GaN crystal structure

Based on the intrinsic property of GaN, by incorporating a heterostructure comprising a thin, high electron mobility material layer of Aluminum Gallium Nitride (AlGaN), strain is then introduced at the contact, producing a two-dimensional electron gas (2DEG) that compensates at the interface (Delagebeaudeuf & Linh, 1982). Electrons can be successfully conducted when an electric field is placed over this 2DEG. The confinement of electrons in a narrow area at the interface contributes to the 2DEG's outstanding conductivity. The AlGaN/GaN heterointerface produces a fixed charge stemming from spontaneous and piezoelectric polarization, resulting in a polarization magnitude difference between the layers and an abrupt polarization shift at the interface. The induced charge density can be either positive or negative, leading to the formation of 2DEG or two-dimensional hole gas (2DHG) at the heterointerface to preserve charge neutrality (Nakajima et al., 2010).

GaN HEMT Architectures

The standard configuration of GaN HEMT incorporating a 2DEG channel at the heterojunction is depicted in Figure 3(a) and is commonly referred to as D-GaN HEMT. This device typically operates in an on-state without gate voltage and can be switched off by applying a negative gate bias below the turn-on threshold gate voltage. However, it is crucial to avoid leaving the gate terminal unconnected, as this may inadvertently activate the device and potentially result in catastrophic failure. Generally, GaN HEMTs employed in power converters need to be normally off devices to guarantee safe operation. If the gate driver is deactivated or malfunctions, and its output drops to zero, the HEMT must switch off (Greco et al., 2018).

Given these properties, D-GaN HEMTs are not recommended as independent switches in renewable energy power conversion applications.

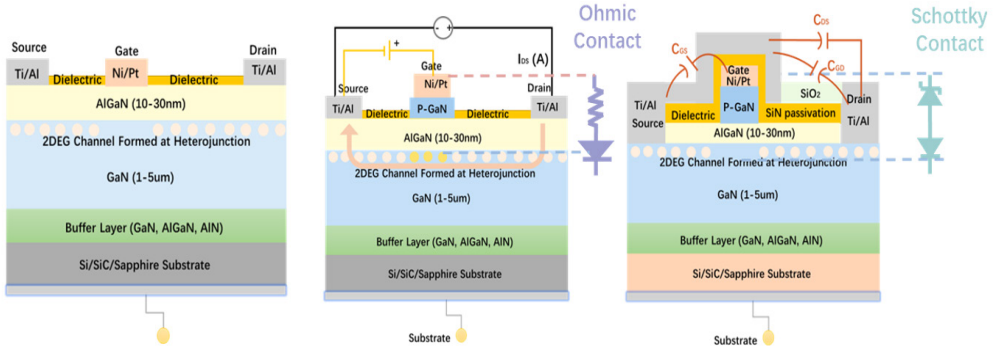


Figure 3. Structure of (a) Conventional GaN HEMT and (b) Gate Injection Transistor (GIT) E-GaN HEMT and (c) EPC Schottky type E-GaN HEMT with locating the internal capacitances

As a solution, commercially available configurations of E-GaN HEMTs are illustrated in Figures 3(b) and 3(c). Figure 3(b) presents the conventional cross-sectional representation

of a gate injection transistor (GIT) structure. The 2DEG underlying the gate is efficiently depleted with V_{GS}=0 by adding a p-type GaN layer to the AlGaN barrier layer within the ohmic contact with the Gate. It facilitates efficient hole injection and raises the conduction band energy. It changes the GaN-HEMT into a typically off-E-mode device. According to this method, the p-GaN area must be removed selectively using plasma etching, which might damage the AlGaN surface and worsen the electrical characteristics of the 2DEG in the device access region (Greco et al., 2018). P-type conductivity in GaN has been achieved at both the laboratory and manufacturing levels. A high doping concentration is necessary for the p-type GaN layer. Magnesium (Mg) replaces the Ga lattice and serves as an acceptor when integrated into the nitrogen lattice, making it the conventional p-type dopant for GaN and AlGaN. Many leading manufacturers, such as GaN Systems Inc., have adopted this structure.

The Schottky-type p-GaN configuration shown in Figure 3(c) also attains a normally off-device operation. Under this structure, the p-GaN layer forms a Schottky contact with the gate metal. This design also incorporates dielectric and passivation layers to insulate the gate, which is deposited on P-GaN and insulated from other contacts. This interlayer dielectric deposition methodology substantially enhances the insulation between the gate and source, improving device stability (Chen et al., 2017). While C_{DS} stands for the effective capacitance between the drain terminal and the field plate, C_{GS} indicates the effective capacitance seen from the channel created by the 2DEG to the field plate atop the gate terminal. Finally, C_{GD} is less significant in size than C_{GS} and C_{DS}, which is in a modest area of the gate terminal. These E-GaN HEMTs display diminished vulnerability to unwanted transient dv/dt voltage spikes, which have the potential to cause unintended turn-on at the transistor's gate terminal, owing to the larger magnitude of C_{GS} in comparison to C_{GD}.

E-GaN HEMT as Power Switching Devices

The E-GaN HEMT devices operate as critical current and voltage switches in the energy system, aiming at power conversion applications. Therefore, the transient switching characteristics of these devices are significant in determining power conversion efficiency (PCE) and high-power performance, which are critical aspects influencing their high-performance capabilities. The parasitic nonlinear junction capacitances affect the switching dynamics of the power electronics device. Key capacitances encompass the input capacitance (C_{ISS}), output capacitance (C_{OSS}), and reverse transfer capacitance (C_{RSS}) (Zhang et al., 2018). These capacitances are correlated with the internal capacitances of the E-GaN HEMTS demonstrated in Figure 3(c), as the Equations 4, 5 and 6 (Wang et al., 2020).

$$C_{ISS} = C_{GS} + C_{GD} \quad [4]$$

$$C_{OSS} = C_{DS} + C_{GD} \quad [5]$$

$$C_{RSS} = C_{GD} \quad [6]$$

Parasitic capacitances are essential for determining switching losses and evaluating gate driver performance in power-switching devices. These parameters are accounted for in the corresponding model in relation to the SPICE models derived from manufacturers.

GaN HEMT Spice Modeling

The dynamic characterization of HEMT switching behavior or power conversion-oriented circuit design requires a double-pulse tester (DPT) circuit with PCB featuring various topologies. However, transient analysis of these devices, particularly GaN HEMTs, can be challenging due to the nanosecond testing intervals when the gate pulse frequency reaches GHz levels, demanding advanced testing equipment. Therefore, electronic simulations are typically employed for efficient pre-experimental circuit design assessment. Simulation Program with Integrated Circuit Emphasis (SPICE), a widely used circuit simulation platform, provides a solution for analyzing and designing complex electronic circuits. The E-GaN HEMT equivalent sub-circuit, illustrated in Figure 4, normally includes a .lib file provided by the manufacturer containing all necessary SPICE model settings. The model comprises a voltage-dependent current source (I_{DS}), three voltage-dependent capacitances (C_{GD}, C_{DS}, and C_{GS}), and three parasitic resistances (R_G, R_S, and R_D). I_{DS} models the static I-V characteristics for both forward and reverse conduction. The parasitic capacitances significantly influence the device's switching performance, while R_G, a relatively small constant, often helps reduce transient oscillations during switching events. R_D and R_S are temperature-dependent resistances representing the terminal topology's distributed nature. EPC and GaN Systems provide E-GaN HEMT SPICE models, with GaN Systems also including thermal resistance connector pins for temperature measurements.

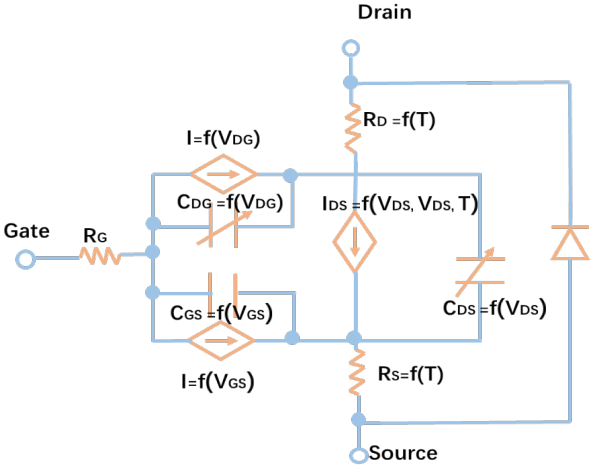


Figure 4. SPICE equivalent of E-GaN HEMT sub-circuit

Parasitic Inductances of E-GaN HEMT

The SPICE model adeptly simulates HEMT switching dynamics, facilitating the study of transient waveforms. However, achieving precise simulation results akin to real-world tests necessitates considering external variables, such as parasitic inductance-induced oscillations. Parasitic inductances in E-GaN HEMTs, undesirable byproducts of device design and assembly, can instigate detrimental outcomes like transient voltage spikes and electromagnetic interference. The primary parasitic inductance sources in E-GaN HEMTs encompass internal device inductance, originating from intra-device current paths, and packaging inductance, stemming from device packaging and interconnections. External inductance, related to device and circuit interconnections, also contributes significantly (Liu et al., 2014). This study chiefly concentrates on internal device and packaging inductance to analyze HEMT switching characteristics at the device level.

METHODOLOGY

The objectives of the simulation design encompass three key aspects: (1) examining the static characteristics of the device, (2) assessing the enhancement in power efficiency through double pulse testing while scrutinizing the switching transients, such as V_{DS}, I_D, V_{GS}, and instantaneous switching power losses in comparison to MOSFETs, and (3) evaluating the influence of parasitic inductance on the switching behavior of the device. The simulation process employs LTSPICE as the software, utilizing the EPC2204 GaN E-HEMT model provided by Efficient Power Conversion (EPC). To facilitate a comparison of switching performance and power loss conditions, the IPA086N10N3 MOSFET is also selected for analysis.

Table 1 presents a silicon FET and a GaN E-HEMT chosen for a performance comparison based on their similar voltage V_{DS} and drain-source on-state resistance $R_{DS(on)}$ ratings. It is crucial to underscore that the GaN E-HEMT has a maximum gate voltage limitation of 6V, substantially lower than the 20V limit of the silicon FET, due to its smaller gate threshold. This characteristic makes gate voltage control more challenging and renders the transistor susceptible to damage should the gate voltage exceed this limitation during peak overshoots or oscillations.

Table 1
Key parameters of silicon and E-Gan FETs

FET Types	Part Number	V_{DS} (V)	I_{DS} (A)	$R_{DS(on)}$ (mΩ)	Q_G (nC)	V_{GS} (V)
E-GaN FET	EPC2204	100	29	6	5.7	-4/6
MOSFET	IPA086N10N3	100	45	8.6	42	±20

Static simulations of the GaN HEMT were conducted based on the detailed parameter settings presented in Table 2. The results are presented in Figure 5. Figure 5(a) illustrates the output characteristics elucidating the relationship between the drain current (I_D) and the forward directional drain-to-source voltage (V_{DS}) under varying gate-to-source voltage (V_{GS}) conditions. Figure 5(b) portrays the static on-resistance in the linear drain current region. Figure 5(c) depicts the typical transfer characteristics, accentuating the variations in I_D across different junction temperatures. It is observable that an elevation in junction temperature yields a reduction in current, attributable to amplified lattice vibrations and diminished charge carrier mobility. Additionally, a subtle yet discernible shift in the threshold voltage is noted. Figure 5(d) presents the reversed curves of I_D-V_{DS} for various V_{GS} levels. Notably, when the freewheeling current I_D = -20A, adjusting V_{GS} from -4V to 6V reduces the on-state V_{DS} magnitude from 6.4V to 0.2V. Distinct from P-N junction reverse bias, the GaN HEMT exhibits resistive behavior through the formation of 2DEG, resulting in tangible losses and indicating substantial reverse conduction losses in power circuit applications. Minimizing reverse conduction loss is advisable, potentially achieved by optimizing the dead time between turning off one switch and turning on another to diminish shoot-through currents and related losses (Niu et al., 2018).

Table 2
EPC 2204 static simulation parameters

Forward Output characteristics	Static On-Resistance R_{ON}	Transfer Characteristics	Reverse Output Characteristics
DC Sweep Junction Temperature: 25°C Type of sweep: Linear 1st source: V_{DS}; Start value:0V; Stop value: 6V; Increment: 0.2V 2nd source: V_{GS}; Start value:1V; Stop value:6V; Increment: 1V	DC Sweep Junction Temperature: 25°C Type of sweep: Linear 1st source: V_{DS}; Start value:0V; Stop value: 6V; Increment: 0.2V 2nd source: V_{GS}; Start value:3V; Stop value:6V; Increment: 1V	DC Sweep Junction Temperature: Step up of 25°C, 75°C, 125°C, accordingly Type of sweep: Linear 1st source: V_{GS}; Start value:-2V; Stop value: 10V; Increment: 0.2V	DC Sweep Junction Temperature: 25°C Type of sweep: Linear 1st source: V_{DS}; Start value:-10V; Stop value: 2V; Increment: 0.2V 2nd source: V_{GS}; Start value:-4V; Stop value:6V; Increment: 2V

DPT Circuit Design for Switching Performance Analysis

The switching performance of GaN HEMT and MOSFET is evaluated using a DPT circuit, which includes a DC power source, a double pole switch, a gate driver circuit, the device under test (DUT), an inductive load, and clamping circuits. An RC snubber circuit

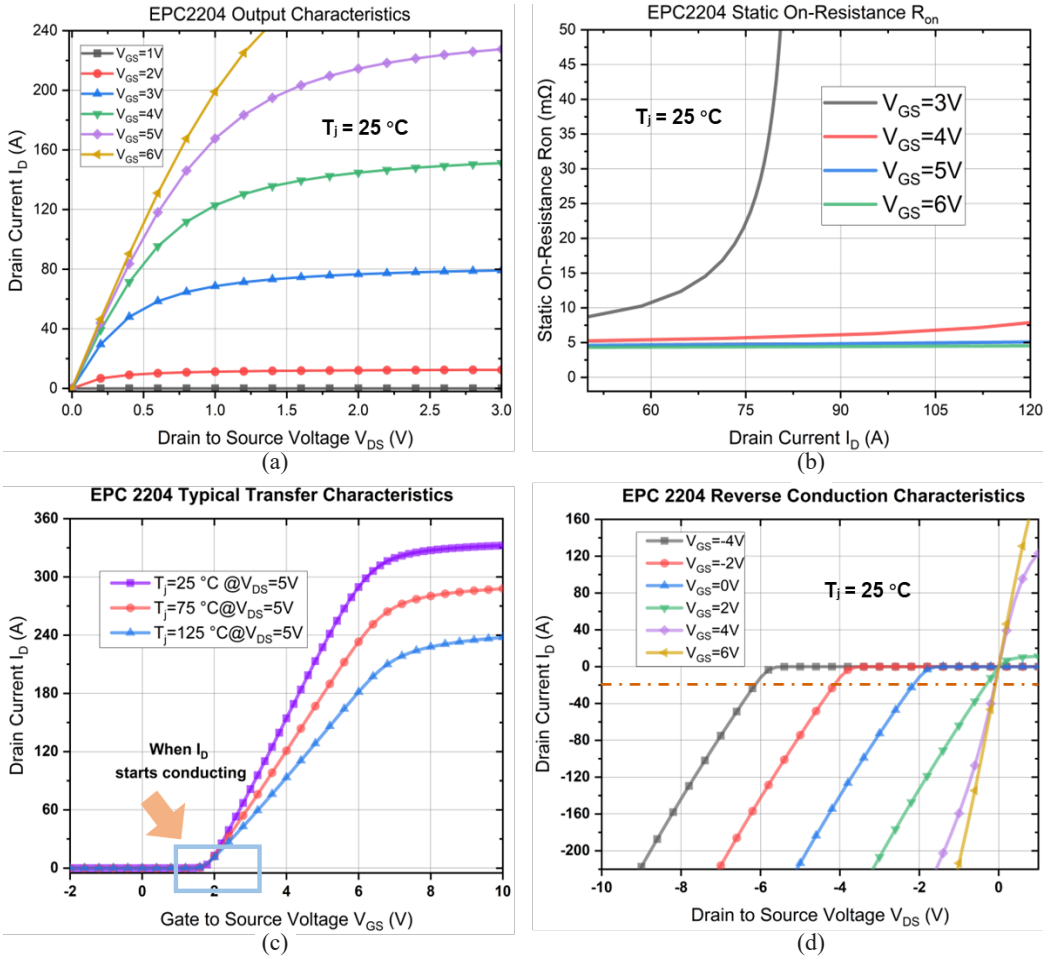


Figure 5. EPC2204 HEMT static analysis: (a) forward output characteristics, (b) static on-resistance R_{on} during linear current region, (c) typical transfer characteristics with junction temperature variation, and (d) reverse output characteristics

is also incorporated to mitigate oscillations from parasitic inductances and capacitances during high-speed switching (Wang et al., 2021). Bulk capacitance maintains a consistent DC voltage across the power supply, preventing sudden DUT switching that could cause voltage oscillations. A decoupling capacitor filters high-frequency noise that rapid DUT switching might generate, ensuring accurate measurements.

Figure 6 presents the LTSPICE schematic employed for the specified simulation. The EPC2204 GaN HEMT is assessed alongside the IPA086N10N3 MOSFET as the DUT while implementing the LTC7001 gate driver. Subsequently, external parasitic inductances, including L_{gs}, L_{ds}, and L_{cm} (Common-Mode Inductance) originating from package inductance, PCB trace inductance, and ground plane inductance, are considered (Jiang et al., 2022). Additionally, stray capacitances emerging from the physical structure of the device,

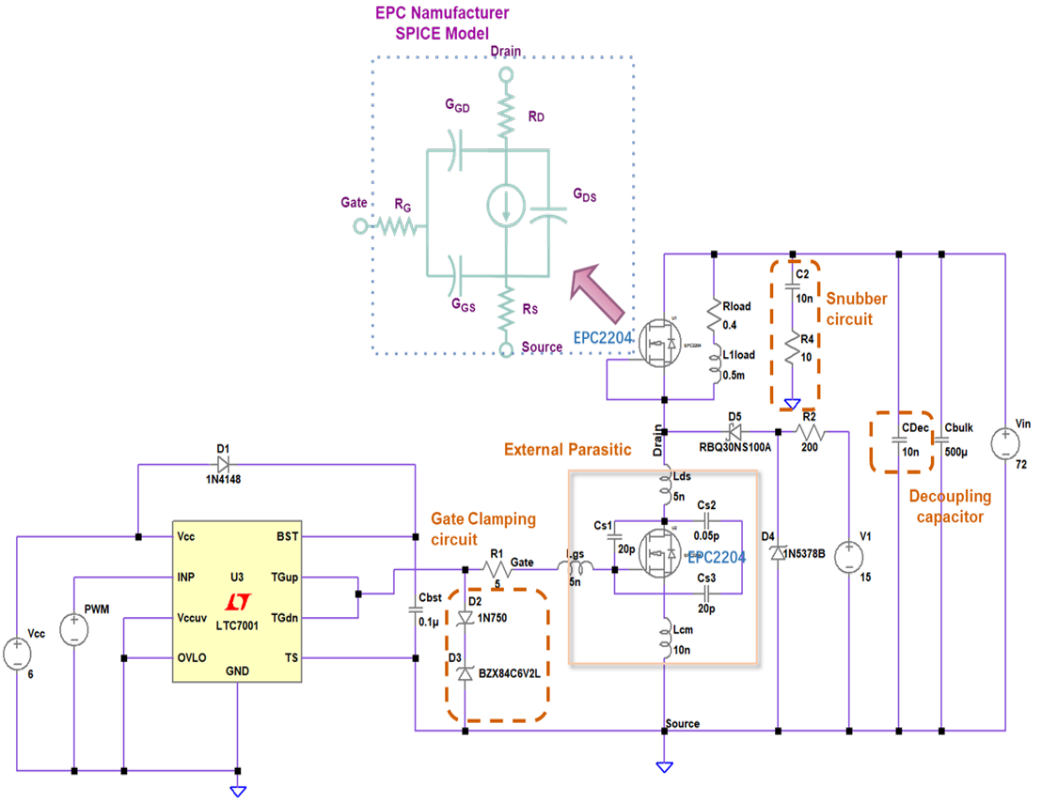


Figure 6. LTSPICE simulation schematic of the proposed DPT circuit with external parasitic

its packaging, and adjacent circuit components are incorporated and simulated, referencing values from prior research. The I_D and V_{DS} transit waveforms between the ideal and parasitic conditions are evaluated. Ultimately, an RC snubber circuit is integrated to evaluate its efficacy in mitigating switching oscillations, as evidenced through waveform comparison (Nakajima et al., 2008). For optimal voltage overshoot attenuation, the snubber capacitor must strike a balance: sufficiently large and perceptive in energy dissipation. Given the EPC2204's C_{OSS} under 1nF, a 10nF capacitor is chosen for simulations. The resistor, tasked with dissipating energy from the snubber capacitor, necessitates suitable value selection depending on load inductance and snubber capacitance. Simulative iterations lead to the selection of a 10-ohm resistor.

RESULTS AND DISCUSSION

The transient simulation parameters are detailed in Table 3. Under ideal conditions, free of external parasitic influences, the turn-on and turn-off transitions of the EPC2204 GaN HEMT and IPA086N10N3 MOSFET are examined in a single cycle, as depicted in Figure 7. LTC7001 filtered gate signal generated full switching-on gate voltages of 5.4V for the EPC2204 GaN HEMT and 8.3V for the IPA086N10N3 MOSFET.

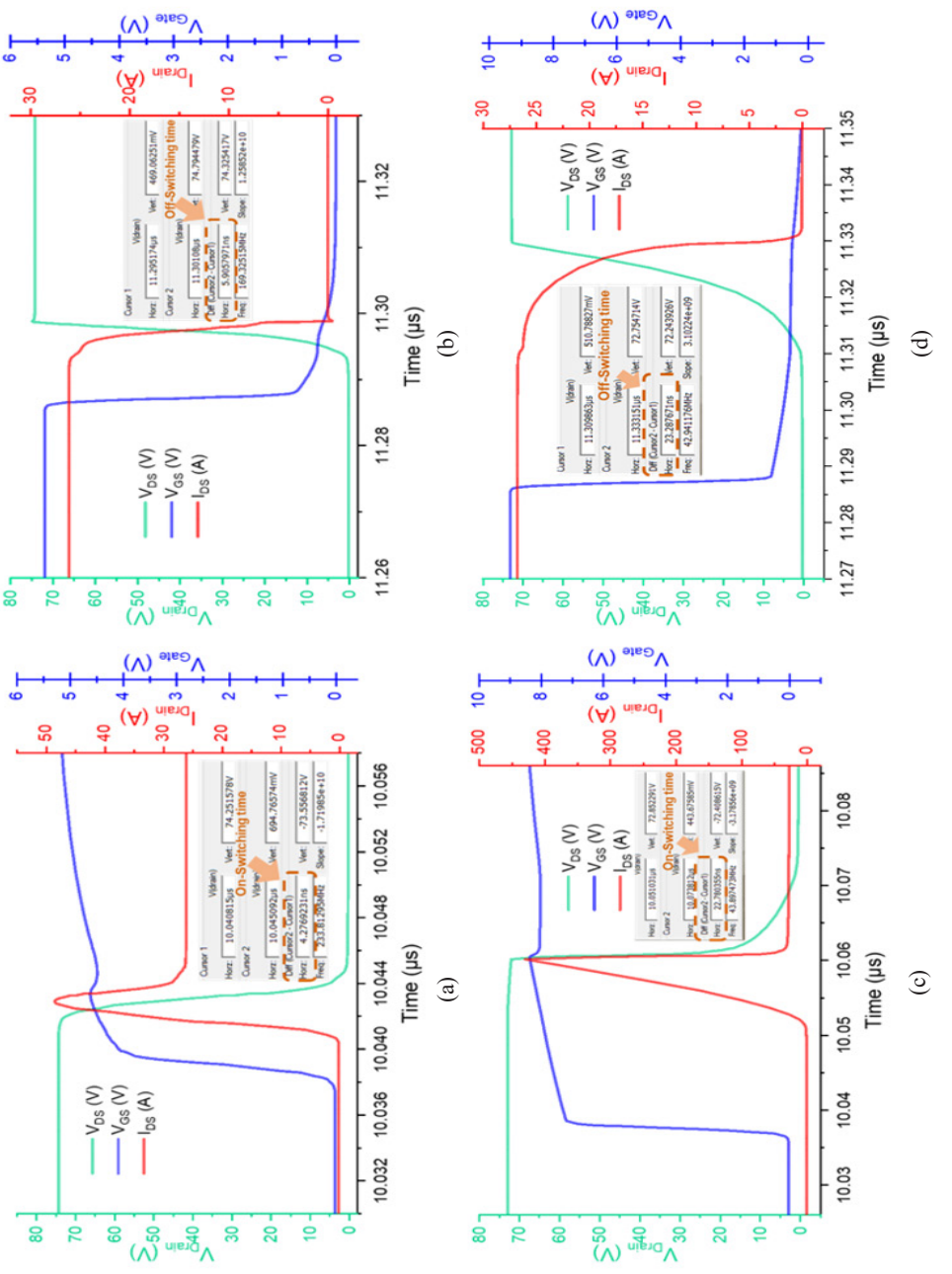


Figure 7. DUT On-switching and off-switching waveforms with R_L=1.3 Ω, L_L=0.75 mH, V_{in}=72 V for (a) EPC 2204 GaN HEMT and (b) IPA086N10N3 MOSFET

Table 3
Simulation settings for hard switching transient analysis

EPC2204 E-GaN FET	IPA086N10N3 MOSFET
PWM pulse setting: $V_{initial}$=-4V; V_{on}=6V;T_{delay}=0; T_{rise}=1ns; T_{fall}=1ns; $T_{(on)}$=1.25µs; $T_{period(s)}$=2.5µs; f_{sw}= 0.4 MHz Stray capacitance: C_{S1}=20pF;C_{S2}=0.05pF; C_{S3}=20pF; External parasitic inductance: L_{CM}=10nH; L_{GS}=5nH; L_{DS}=5nH	PWM pulse setting: $V_{initial}$=-10V; Von=10V;Tdelay=0, T_{rise}=1ns; T_{fall}=1ns; $T_{(on)}$=1.25µs; $T_{period(s)}$=2.5µs; f_{sw}= 0.4 MHz
Power Setting: V_{in}=72V; L_{load}=0.75mH; R_{Load}=1.3Ω Gate driver: LTC7001; Transient stop time: 2ms; Time to start saving data: 1.98m; Maximum time step: 1µs	

According to Figure 7(a), under the specified load parameters (R_L=1.3 Ω, L_L=0.75 mH) and an input voltage of V_{in}=72 V, approximating the output of two series-connected solar panels under open-circuit voltage (V_{OC}) conditions, the GaN HEMT displayed a transient current spike of 49 A before reverting to a load current of 26A. This transition was characterized by smooth oscillatory curves that helped mitigate current overshoot. The entire turn-on phase lasted 4.28ns, while the turn-off phase took 5.91ns. Conversely, as per Figure 7(b), the current in the MOSFET spiked sharply to 445A during the switching-on process before abruptly falling to the load current. The respective durations of the on-and-off switching processes were 22.8ns and 23.3ns. The data reveals that the GaN HEMT's on-and-off switching responses were 5.3 and 3.9 times faster.

Apart from the exceptional switching time and relatively minor current spike, the GaN HEMT surpasses the MOSFET in switching power losses for the DUTs under DPT. As shown in Figure 8(a), the waterfall plot highlights the maximum peak instantaneous power losses for both the GaN HEMT and MOSFET, representing the sum of the product of gate voltage and gate current, as well as the product of drain voltage and drain current. Notably, there is a significant difference in the magnitude of switching power losses between the two devices. The MOSFET's highest instantaneous power losses reach 16,000 W, while the GaN HEMT dissipates approximately 3,000 W within a nanosecond interval. With respect to off-switching power losses, the MOSFET dissipates nearly 580 W. At the same time, the GaN HEMT exhibits a peak power of 530 W. Figures 8(b) and 8(c) present a comparison of average power losses, calculated by integrating the area and dividing by the time interval. The GaN HEMT delivers a remarkable reduction in switching power loss for both on and off-half cycles. Those advantages of lower instantaneous peak current and quicker switching times, as well as reduced switching power losses, can be ascribed to GaN's inherently higher electron mobility, diminished C_{OSS}, reduced gate charge and Miller charge, which further underscore GaN's superiority in hard-switching power conversion applications.

Figure 8(d) validates the simulation results against empirical data and pertinent literature. Given the multitude of dependent variables in actual power conversion applications, such as switching frequency, circuit topology, and switching mode (hard or soft switching), data are grouped and compared under identical conditions. Under a non-isolated, hard-switching 48V-12V buck converter condition, the E-GaN HEMT demonstrates superior efficiency in load regions exceeding 50W (Reusch et al., 2015). Analogous conclusions are drawn from isolated ZVS 400V-14V full-bridge topology (Kim et al., 2015). This data underscores the generalized superiority of E-GaN HEMT over MOSFET across various power conversion applications.

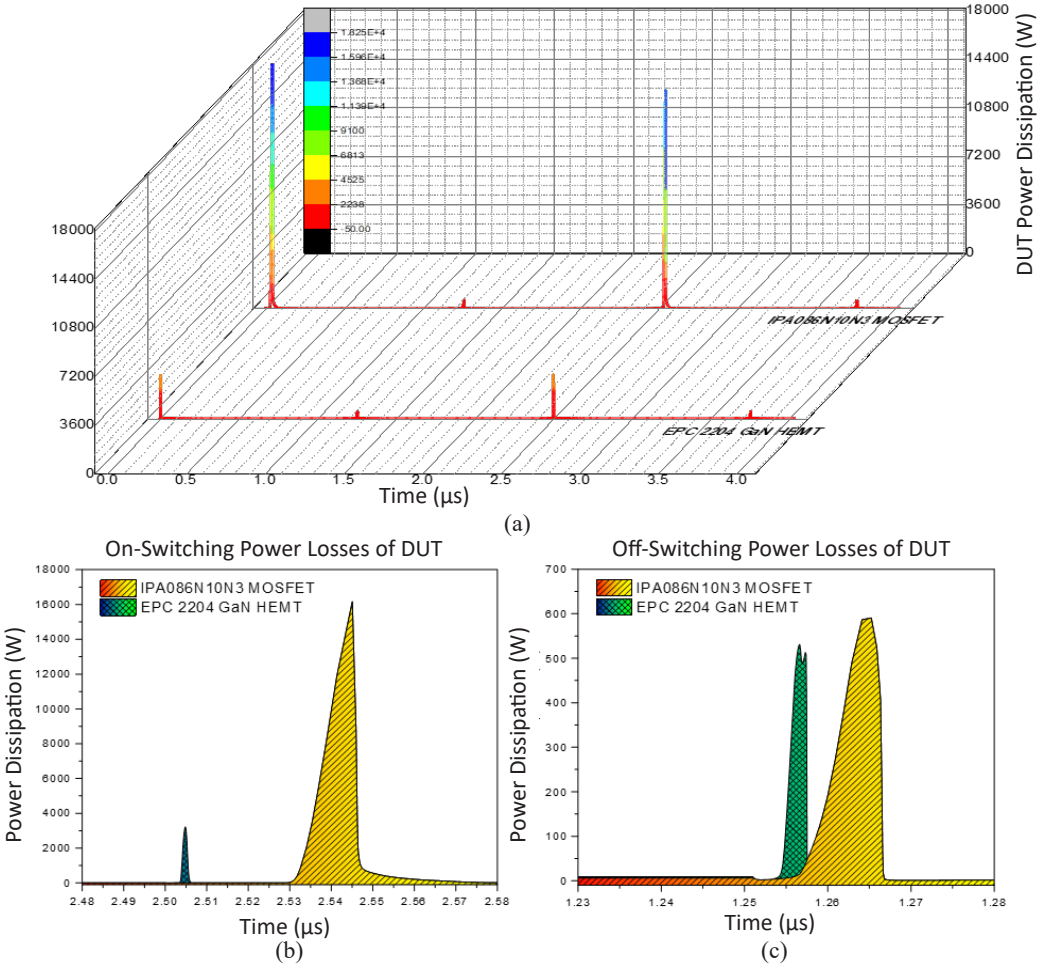
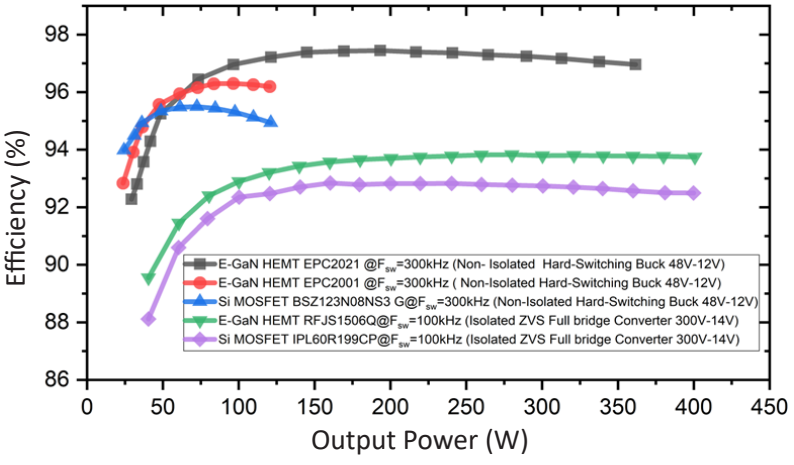


Figure 8. (a) waterfall plot of power device losses in two cycles, (b) DUT on-switching power losses comparison, (c) DUT off-switching power losses comparison,



(d)

Figure 8. (Continue) (d) validation of efficiency enhancement through comparison with existing research findings

Examining E-GaN HEMT Solutions for Improved Threshold Voltage Stability

Despite the superior switching behavior and reduced power losses associated with E-GaN HEMT, DC analysis reveals a notable imperfection: a narrow gate voltage threshold. This occurrence might lead to challenges in gate pulse control and, in some cases, even failure. As illustrated in Figure 9, upon initiating hard switching of EPC2204 E-GaN HEMT, I_D begins to conduct when $V_{GS(ON)}$ reaches 1.70 V, while its switching off process at a $V_{GS(OFF)}$ of 2.25V. In synchronous DC-DC converter designs, the gate pulse for one switching device is customarily the logical inverse of the other's pulse signal. Given the prevailing challenges associated with a low gate threshold voltage, an extended dead time is necessary to preclude both transistors' concurrent activation within a half-bridge topology. Inadequate deadtime management can exacerbate losses and jeopardize the device's integrity, potentially compromising the circuit's stability.

A solution to address the imperfections of E-GaN HEMTs involves applying cascading GaN HEMTs. This configuration involves the series connection of a low-voltage silicon MOSFET with the GaN HEMT, where the silicon MOSFET serves as a level shifter to regulate the gate voltage of the GaN device, preventing it from surpassing its threshold voltage. This configuration effectively mitigates the issue of gate leakage current that is often associated with standalone E-GaN HEMTs. Nonetheless, challenges related to packaging parasitics and associated costs persist.

An alternative approach involves adapting the gate driver to provide meticulous control over the gate voltage. The integration of the LTC7001 gate driver, which generates robust pull-up and pull-down currents to the gate of GaN HEMT and precisely controls the temporal lag between the gate pulse signal and HEMT drain response, introduces a delay

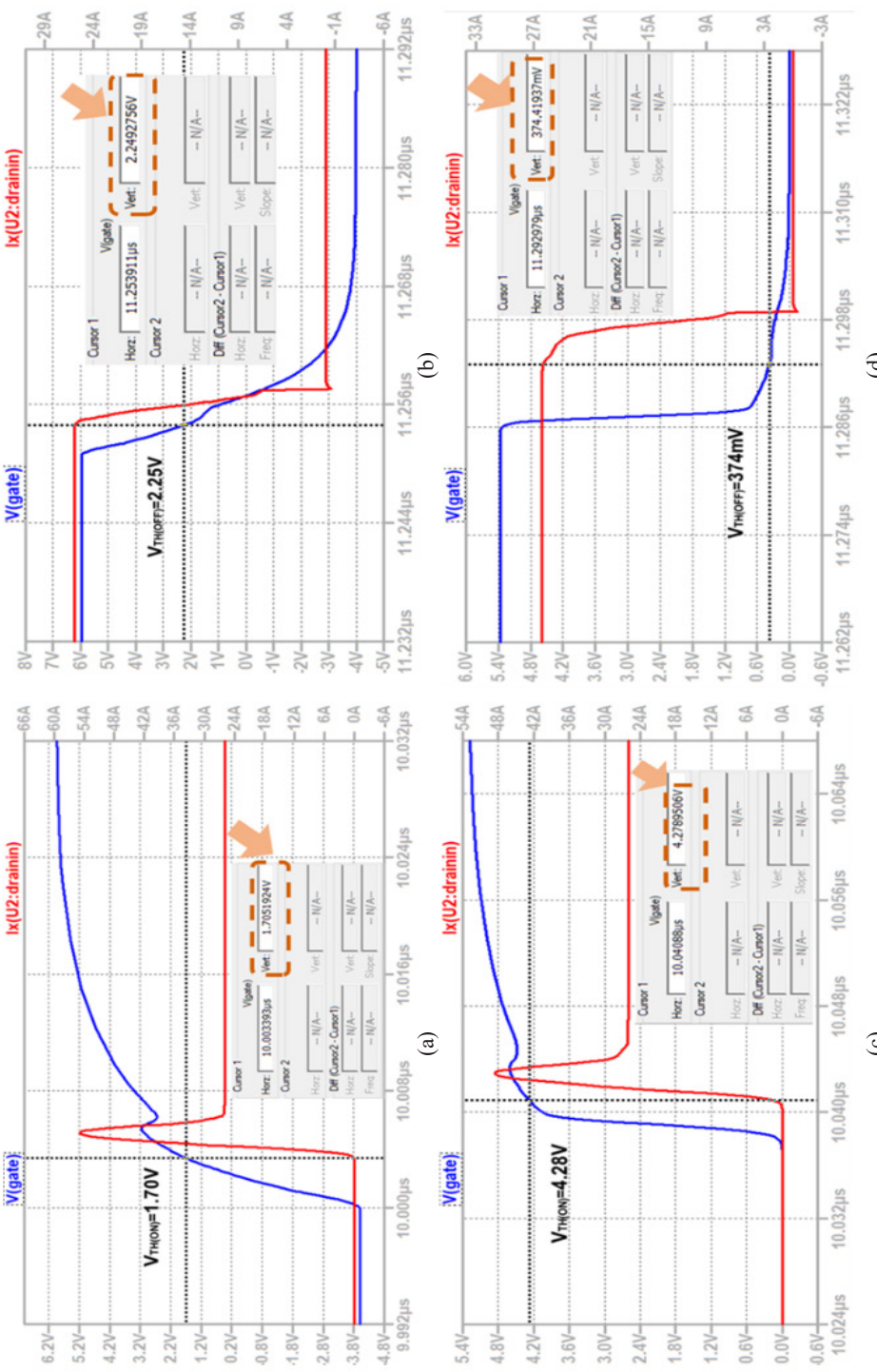


Figure 9. Observation of EPC2204 E-GaN HEMT threshold gate voltage under (a) turning-on without LTC7001, (b) turning-off without LTC7001, (c) turning-on with gate signal processed by LTC7001, and (d) turning-off with gate signal processed by LTC7001

to both on-switching and off-switching processes. This delay significantly mitigates the aforementioned issues. Figure 9(c) illustrates that when the HEMT initiates the turn-on process, the gate voltage reaches 4.28 V, aligning closely with the upper threshold gate voltage in the linear and saturation region. Conversely, when the HEMT begins the off-switching process, the gate voltage has already dropped to 0.374 V. This advancement effectively eliminates the crosstalk of gate signals between the two transistors of the synchronous converter.

Influences of Parasitic Inductances and Stray Capacitances

While the EPC2204 E-GaN HEMT exhibits optimal performance characteristics, such as faster switching speed, fewer current spikes, and reduced power losses, its operation under LTSPICE simulation, which considers internal capacitance and parasitic resistances only, is significantly influenced by parasitic inductances and stray capacitances, as discussed before. This influence becomes apparent in Figures 10(a) and (b), where substantial oscillations are seen in V_{GS}, V_{DS}, and I_D. Dense oscillations are followed by a second set of oscillation

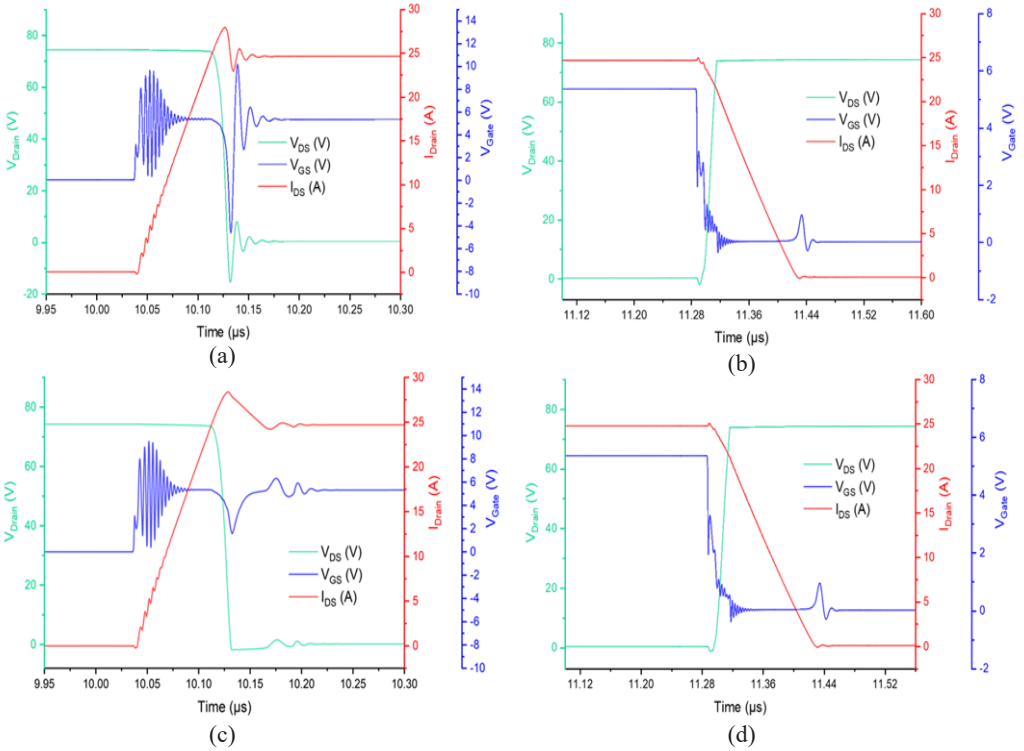


Figure 10. Influences of Parasitic Inductances and Stray Capacitances for GaN HEMT during (a) on-switching without clamping and snubber circuit, (b) off-switching without clamping and snubber circuit, (c) on-switching within clamping and snubber circuit and (d) off-switching within clamping and snubber circuit

spikes that range from -5V to +10V, beginning with the gate pulse. This range surpasses the maximum gate threshold of EPC2204 (-4V to +6V) and could potentially lead to device damage. Furthermore, the initial V_{DS} spikes exhibit a high negative value of -17V, indicative of a reverse bias condition. This negative bias could also lead to power loss and potential functional discrepancies in the circuit. Although the peak overshoot in I_D appears to be lower, the duration of oscillations increases the overall switching speed, potentially compromising the stability of constant current output for DC-DC converter applications.

These parasitic effects can be mitigated by integrating snubber and clamping circuits for gate-source and drain-source, as depicted in Figures 10(c) and (d). The gate-source clamping circuit, which incorporates a reverse-connected zener diode with a rated voltage identical to the maximum threshold of the GaN HEMT gate, truncates the peak overshoot and buffers the oscillation. Regarding V_{DS}, the negative spike is eliminated by the drain-source clamping circuit, in addition to the buffered I_D oscillation waveform, which enhances current stability. It is also observed that the gate oscillation magnitude is reduced during the off-switching cycle. In addition, when designing HEMT circuits, it is essential to minimize parasitic inductances and stray capacitances by optimizing the layout and routings of the PCB.

CONCLUSION

In this study, a detailed examination of the E-GaN HEMT was undertaken, particularly focusing on its 2DEG output property, which differentiates it from traditional P-N junction devices. The unique behavior of this 2DEG semiconducting property was characterized through static DC analysis. A comparative hard-switching transient simulation was conducted using a half-bridge circuit schematic, highlighting the pronounced performance of GaN over MOSFET in power converter applications. This superior performance is attributed to the absence of reverse conduction losses inherent to the 2DEG characteristic and reduced output capacitances due to device size and packaging considerations. Furthermore, the influences of external parasitic inductances and stray capacitances on transient performances were examined, offering insights for PCB design in real-world applications. The findings underscore the potential of E-GaN HEMTs to enhance the efficiency of DC-DC converters, particularly for photovoltaic energy delivery.

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